Add-on Extension for EDA Users

Design for Reliability

Ensure Your Electronic Design is Reliable and Robust During Schematic, Before Layout, Testing and Manufacturing

Using Simulation and Circuit Analysis which Detect Design Errors
A world leader in Reliability & Maintenance Engineering (RAMST) solutions for the EDA market

Founded in Israel in 1989 as a Consulting and Software development company for implementing RAMST

Until today BQR performed ~3500 projects

BQR team includes experts in:
Mathematics, Electronics and Reliability engineering

Worldwide customers including leading global enterprises
BQR Software Products

Eliminate Design Errors in Advance
fiXtress™
Chip, Board & System Level
Design Error Detection & Electrical Stress Analysis

Enhance Product Reliability & Safety
CARE®
System Level
Computer Aided Reliability Engineering

Reduce Maintenance Costs
apmOptimizer™
Asset & Fleet Level
Maintenance Planning & Optimization
Detailed Modules list

**fiXtress**
for Electronics
Single and Multi Boards

- **ASR** Automated Schematic Review
  - Driven by Electrical Stress analysis
  - Common ready to use Rules
  - User defined Rules
  - Hierarchic and Grouped Rules for Chips and BUS Interconnection

- **ASA** Automated Electrical Stress Analysis
  - **Rapid** DC Stress Analysis
  - **Precise** DC/AC Stress Simulation
  - **Thermal Analysis**
  - **Stress Derating Analysis**

- **MTBF** Mean Time Between Failures
  - **Basic** BOM calculation
  - **Pro** BOM + Stress calculation

**CARE**
Computer Aided Reliability Engineering
Including Safety Analysis for Electronic and Mechanical Systems

- **FME(C)A** Failure Modes Effects Analysis
- **TA** Testability (Built-In/Self Test) Analysis
- **FTA** Fault Tree Analysis (Safety Analysis)
- **RBD** Reliability/Redundancy Block Diagram
  - Basic (Parallel, K out of N, Stand-By)
  - Markov (States Transition Model)
  - Network
  - IEC-61508 (Safety Analysis)

**apmOptimizer**
Asset Performance Maintenance Optimizer
Planning and Real Time Optimization

- **LCC** Life Cycle Cost, Operation & Maintenance Model
  - Asset Availability & Reliability analysis
- **LORA** Level Of Repair Analysis & Optimization
- **Predictive** Maintenance Optimization
- **Spare** Parts Inventory Optimization
- **RO** Resources Optimization
  - (Manpower, Tools & Materials)
- **RCM** Reliability Centered Maintenance
- **MSG-3** Aerospace Maintenance Steering Group
- **FDA** Field Data Analysis
  - Real time maintenance records analysis and

**CORE database**
Component/PCB level through System level up to Asset/Fleet level
Typical Products failures

fiXtress™

Will help you to prevent such cases
Standard Design Flow

Design

Schematic

DRC, Visual Inspection

PCB Layout

Prototype Manufacturing

Prototype Test

Qualification Test

Integration Test

Customer

Design Correction

Root Cause Analysis

Found Design Error

$10

$100

$1,000

$10,000

$100,000

$1,000,000
fiXtress Design Flow

ODM Check gate for Design Quality
Original Design Manufacturer

Benefits:
• Saves time of schematic visual inspection
• Saves Design debug time
• Reduces Design Re-Spins
• Improves Documentation and Process
Return on Investment
ROI when failure is detected during testing 1 : 10
ROI when failure is detected by customer 1 : 1000
Statistics on 14 boards

Design errors and stress errors

ROI : 1 - 35

<table>
<thead>
<tr>
<th>Number</th>
<th>Item</th>
<th>PAD Quantity</th>
<th>Components quantity</th>
<th>Net quantity</th>
<th>Finding Errors(*)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Module 1</td>
<td>11238</td>
<td>1691</td>
<td>2315</td>
<td>129</td>
</tr>
<tr>
<td>2</td>
<td>Module 2</td>
<td>8825</td>
<td>1931</td>
<td>2666</td>
<td>51</td>
</tr>
<tr>
<td>3</td>
<td>Module 3</td>
<td>4318</td>
<td>10005</td>
<td>1172</td>
<td>6+35</td>
</tr>
<tr>
<td>4</td>
<td>Module 4</td>
<td>2870</td>
<td>751</td>
<td>749</td>
<td>3+82</td>
</tr>
<tr>
<td>5</td>
<td>Module 5</td>
<td>10169</td>
<td>1395</td>
<td>1139</td>
<td>2+17</td>
</tr>
<tr>
<td>6</td>
<td>Module 6</td>
<td>1190</td>
<td>286</td>
<td>299</td>
<td>3+2</td>
</tr>
<tr>
<td>7</td>
<td>Module 7</td>
<td>7215</td>
<td>1279</td>
<td>1781</td>
<td>24+12</td>
</tr>
<tr>
<td>8</td>
<td>Module 8</td>
<td>6450</td>
<td>1343</td>
<td>1390</td>
<td>21+66</td>
</tr>
<tr>
<td>9</td>
<td>Module 9</td>
<td>9480</td>
<td>979</td>
<td>2192</td>
<td>11+5</td>
</tr>
<tr>
<td>10</td>
<td>Module 10</td>
<td>1963</td>
<td>426</td>
<td>380</td>
<td>6+5</td>
</tr>
<tr>
<td>11</td>
<td>Module 11</td>
<td>6584</td>
<td>749</td>
<td>2014</td>
<td>4+23</td>
</tr>
<tr>
<td>12</td>
<td>Module 12</td>
<td>2657</td>
<td>157</td>
<td>941</td>
<td>1+24</td>
</tr>
<tr>
<td>13</td>
<td>Module 13</td>
<td>3318</td>
<td>697</td>
<td>895</td>
<td>9+3</td>
</tr>
<tr>
<td>14</td>
<td>Module 14</td>
<td>4365</td>
<td>1069</td>
<td>1158</td>
<td>11+50</td>
</tr>
</tbody>
</table>
Design error sample (1)

0.138 V > 0V

“Floating IC GND” rule #2
fiXtress Benefit

- Automated Schematic Review tool; Detect hidden design errors, driven by Electrical Stress, Reliability, Testability and Safety analysis
- fiXtress use the ICD (interface Control Document) signals and their tolerance, this means we do a real stress analysis and schematic review based on the power supplies and loads
- Single and Multi Boards analysis using the ICD between PCBs, if you don’t use the ICD its not a real analysis
- Ready to use 17 groups of design rules, each one about 15 sub-groups (~200 rules)
- User can define easily new design rules for different applications such as Testability, ESD and Safety (ready 56 rules)
- Rules are not scripts which run individually one by one, fiXtress runs all rules together using the results effects between components
- Advanced level of rules that can check group of signals & BUSs between chips
- Check for every pin the applied actual voltage and current, that comes from a real stress analysis to fulfil the components standards
- Prevent hidden design errors, the cause of NFF (No Failure Found) during operation
- Very fast and accurate results in minutes for hundreds of rules on a 100,000 pads PCB with 25,000 components
- Ready to use derating standards
- User can create his own derating standard
- Detect all EOS (Electrical Over Stress) violations with Pareto, overstress and overdesign reports
- Unique Thermal analysis that estimate the average temperature rise over the cold-plate, for accurate stress Derating
- Calculate the accurate MTBF base on real electrical and thermal stress
- MTBF prediction for all available standards
- Drive reliability data automatically to all RAMS analysis (FMECA, FTA, RBD, MTTR)
• Modular product, from simple MTBF prediction up to full electrical simulation:
  • Automated Schematic Review
  • Electrical Stress Analysis
  • Mini Thermal Analysis
  • Components Derating
  • MTBF Prediction
• Runs on single and multi-board systems
• Detects design errors before layout and production
• Helps to easily implement Good Engineering Practice
• Integration with all major EDA tools
• Component Library and wizard to add new components
• Works on any size of mixed analog and digital designs
Benefits

- Helps to design Robust & Reliable Electronic Products
- Shortens the design cycle by 50%
- Saves hardware engineers weeks of:
  - Manual Stress calculations
  - Visual Schematic inspection
  - Lab debug time during system integration
- Shortens design verification time by 90%
- ROI (Return On Investment) from 10 up to 1000
- Helps prime integrators ensure that products designed by ODM (Original Design Manufacturing) are of high quality, reliable and robust
- Improves Documentation and Process
- Allows designers enhanced self-check capabilities
- Supports good engineering practice within the company
The Opportunity for EDA SW Providers

- Add-On software to:
  - Altium, Cadence and Mentor EDA tools
  - Siemens Team-center, Agile PLM/PDM tools
- Increases the vendor products line and value
What is stress?

Max Cable: 500Kg

Max Cable: 2,000Kg

Derating:
25% from max load

After 1,000,000 times the cable will tear
Derating in Electronics

![Diagram showing derating in electronics with power and ambient temperature on axes]
What is Reliability

Failure probability Vs. Temperature and electrical stress
**fiXtress Integrated Flow**

**fiXtress**

- **ASR**
  - Single Board
  - Avoid Errors causing high stress
  - 1. Common
  - 2. Connectivity Verification
  - 3. Chip Interconnection
  - Automated Schematic Review

- **Rapid**
  - Single Board
  - Avoid Errors caused by high stress
  - Stress Simulation
    - Rules Based DC
  - Automated Schematic Review
    - Comply with Electrical Specs

- **Precise**
  - Single Board
  - Avoid Errors caused by high stress
  - Stress Simulation
    - DC, AC & BUS
    - Full Kirchhoff + Fourier
  - Automated Schematic Review
    - Comply with Electrical Specs

- **ASR**
  - Multi Boards Integration

**Back Annotation**

**Schematic Design:**
- BOM
- Net List
- PINs
- ICD

**fiXtress Plug-In & Tool-kit**
- Data Preparation
- MTBF Parts Count
- Net Name Generator

**OrCAD Mentor Graphics**

**fiXtress**

**Delta T Calculation**

**Stress Derating Analysis**
- Stress Derating
- Parts Stress
- MTBF

**MTBF Results Review**

**MTBF**

**Power Voltage Current**

**Integration Effects Review**

**Schematic n**

**Schematic 2**

**Schematic 1**

**Server fiXtress Libraries**
fiXtress Models operation overview
Integration with CAD & PLM Tools

fiXtress Extension

EDA Schematic Capture

Input Files:
- BOM
- Net-List
- Pin-Lib

Results Files:
- MTBF
- SDTA
- Errors Report

fiXtress

Input Data Processing

Output Data Processing

Integration with CAD & PLM Tools

Oracle PDM Agile

Before fiXtress

After fiXtress

MTBF (Hours)

MTBF vs. Temperature Temp. °C
Automated Electrical Stress Analysis

The two most common typical failures in the field are NTF and EOS:

- **NTF** = “No Trouble Found” (“NFF - No Failure Found”)
- **EOS** = “Electrical Over Stress”

**NTF:**
35%-70% of PCBs declared by field technicians as failed, are functional and no failure is found in the lab. This dramatically increases the number of PCBs in the pipeline, causing manufacturers large losses.

**EOS:**
Material damage may occur when an electronic device is subjected to a power, current, voltage or temperature that is beyond the specified limits of the device.

- EOS affects product performance until the component burns. It is the leading cause of returns in components, IC and system failures during operation
- EOS causes damage to the materials, and product recalls, since this design error is embedded in all PCBs in the field.

fiXtress detects all EOS errors while increasing PCB reliability, and saving time and money

**fiXtress solves NTF and EOS problems in a single tool**
Mini Thermal

Calculate the average $\Delta T$ between operation and cold plate modes
Mini Thermal Module

Results are similar to CFD thermal analysis

Ta = 71°C
Perform Electrical Stress Derating Analysis
What Is Stress Derating?

• Stress in electronic parts may refer to Voltage, Power, Current and Junction Temperature.
• Derating increases the safety margin between part design limits and applied stresses, thereby providing extra protection for the part.
• By applying Derating for electronic components, their degradation rate is reduced. The reliability and life expectancy are increased.
MTBF Prediction

Calculate the MTBF of each PCB, and for the entire system
MTBF Prediction: Mean Time Between Failures

Prediction methods:

**Mil-HDBK-217-F2 & G**: Defense, Aerospace & any mission critical usage

**Telcordia Ver.3**: US Telecom

**FIDES**: Airbus

**IEC-62308**: French Telecom

**SN-29500**: Industry

The MTBF prediction result will increase by 50% after using fiXtress.
PCB Power Reduction after Using fiXtress

Before:

After: power was reduced
MTBF Improvement after Using fiXtress

Before design errors correction
Perform multi boards schematic review and stress analysis
Reliability & System Safety Analysis Flow & Tasks from Component, Function, PCB, Box, sub-system, System up to Asset or Fleet Level

**FMECA**
- Build Components / Functional Failure Modes Catalog for Criticality, Safety & Testability Analyses
  - Functional breakdown
  - Failure Modes assignment
  - Next Higher Effect assignment
  - Severity Classification

**Testability**
- Define BIT concept & Tests to calculate BIT Coverage and Isolation
  - Assign for each Failure Mode the Relevant Built-In-Test (BIT)

**FTA**
- Build the Failure Modes Combinations Tree for System Safety Analysis
  - Build for each Safety Event the possible causes
  - Top-Down Assignment of Logical gates

**RBD**
- Build Redundancy model for System Availability Calculations
  - Assignment of required blocks / functions for a mission
  - Define the blocks / functions redundancy model

Integrated CARE Flow

CARE Libraries

fiXtress Boards Results
- PCB 1
- PCB 2
- PCB n

System Integration
FMECA

Build Components / Functional Failure Modes Catalog for Criticality, Safety & Testability Analyses

• Functional breakdown
• Failure Modes assignment
• Next Higher Effect assignment
• Severity Classification
Failure Mode, Effects, and Criticality Analysis (FMECA), Functional Analysis

What is it?
• Bottom-up process of defining failure modes and their effects
• Starting at component or function level, up to system level
• Assign severity of each system level failure
• Calculate Risk Matrix

Why is it important?
• Identify single points of failure before production – Save cost
• Required as part of Functional Safety and risk management standards
  • IEC 61508 - electrical/electronic/programmable electronic
  • ISO 26262 - Automotive
  • IEC 61511 - Process
  • IEC 61513 – Nuclear
  • IEC 62061 – Manufacturing / machinery
• ISO 14971 - Medical

<table>
<thead>
<tr>
<th>Failure Modes Criticality Matrix</th>
<th>Quantity for Internal Causes only</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part of Overall Criticality</td>
<td>SEVERITY</td>
</tr>
<tr>
<td>Group</td>
<td>Absolute Range</td>
</tr>
<tr>
<td>a</td>
<td>b</td>
</tr>
<tr>
<td>A</td>
<td>4.63815e-005 - 0.000231908</td>
</tr>
<tr>
<td>B</td>
<td>2.31908e-005 - 4.63815e-005</td>
</tr>
<tr>
<td>C</td>
<td>2.31908e-006 - 2.31908e-005</td>
</tr>
<tr>
<td>D</td>
<td>2.31908e-007 - 2.31908e-006</td>
</tr>
<tr>
<td>E</td>
<td>0 - 2.31908e-007</td>
</tr>
</tbody>
</table>
Failure Mode, Effects and Criticality Analysis

Build Components / Functional Failure Modes Catalog for Criticality, Safety & Testability Analysis

• Functional breakdown
• Failure modes assignment
• Next higher effect assignment
• Severity classification

<table>
<thead>
<tr>
<th>Region</th>
<th>Sev</th>
<th>Prob. Group</th>
<th>Block ID</th>
<th>Ref/Desc</th>
<th>Function</th>
<th>Description</th>
<th>Failure Mode ID</th>
<th>Failure Mode Name</th>
<th>Criticality Co.</th>
<th>Probability</th>
<th>Criticality Ratio for Severity</th>
<th>Criticality Ratio from System</th>
<th>Detection Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>7</td>
<td>C</td>
<td>A1</td>
<td>Power Filter</td>
<td>-</td>
<td>A1_02, Filter Output Power below min</td>
<td>1.1537E-005</td>
<td>1.1537E-005</td>
<td>0.073309</td>
<td>0.036361</td>
<td>5</td>
<td>3, 4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td>A1_01, No Filter Output Power</td>
<td>3.790E-006</td>
<td>3.790E-006</td>
<td>0.013851</td>
<td>0.063140</td>
<td>5</td>
<td>3, 4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>3</td>
<td></td>
<td>B1</td>
<td>Input Signal Circuit</td>
<td>-</td>
<td>Input Signal Circuit</td>
<td>62</td>
<td>No Signal from Encoder</td>
<td>5.0X31E-005</td>
<td>5.0X2E-005</td>
<td>0.251807</td>
<td>0.218325</td>
<td>3, 5</td>
</tr>
<tr>
<td></td>
<td>33</td>
<td></td>
<td>B</td>
<td>ADC</td>
<td>-</td>
<td>ADC</td>
<td>86</td>
<td>Bad ADC Data</td>
<td>2.5952E-005</td>
<td>2.5953E-005</td>
<td>0.129093</td>
<td>0.111001</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>33</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>85</td>
<td>No ADC Data</td>
<td>2.5952E-005</td>
<td>2.5953E-005</td>
<td>0.129093</td>
<td>0.111001</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td></td>
<td>B</td>
<td>Input Clock Circuit</td>
<td>-</td>
<td>Input Clock Circuit</td>
<td>53</td>
<td>No Sampling Clock</td>
<td>1.078E-005</td>
<td>1.078E-005</td>
<td>0.035456</td>
<td>0.046309</td>
<td>3, 5</td>
</tr>
<tr>
<td></td>
<td>33</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>63</td>
<td>Bad Signal from Encoder</td>
<td>2.1098E-005</td>
<td>2.1098E-005</td>
<td>0.109349</td>
<td>0.093668</td>
<td>3, 4, 5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>33</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>87</td>
<td>Bad ADC Configuration</td>
<td>2.976E-005</td>
<td>2.976E-005</td>
<td>0.048547</td>
<td>0.035924</td>
<td>6, 5</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td></td>
<td>C</td>
<td>LVDS Receiver Block</td>
<td>-</td>
<td>LVDS Receiver Block</td>
<td>123</td>
<td>Wrong LVDS Data</td>
<td>2.0242E-005</td>
<td>2.0242E-005</td>
<td>0.109095</td>
<td>0.087284</td>
<td>3, 5</td>
</tr>
<tr>
<td></td>
<td>33</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>54</td>
<td>Noisy Sampling Clock</td>
<td>2.5074E-005</td>
<td>2.5074E-005</td>
<td>0.081212</td>
<td>0.100015</td>
<td>6, 5</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td></td>
<td>D</td>
<td>Serial EEPROM Block</td>
<td>-</td>
<td>Serial EEPROM Block</td>
<td>147</td>
<td>Wrong EEPROM Data</td>
<td>7.4010E-007</td>
<td>7.4010E-007</td>
<td>0.029007</td>
<td>0.0301002</td>
<td>6</td>
</tr>
</tbody>
</table>

Reliability Critical Failure Mode List (Full Report for Internal Causes only)
Failure Mode, Effects and Criticality Analysis: Failure Mode Effect Propagation

Failure Effect: Consequence of block failure

Simple path

Block

Failure mode
Failure Effect: consequence of block failure

Simple path
Failure Mode, Effects and Criticality Analysis: Failure Mode Effect Propagation

Failure Effect: Consequence of block failure

- Path with sibling effect
Failure Mode, Effects and Criticality Analysis: Failure Mode Effect Propagation

Failure Effect: Consequence of block failure

- Summing failure rates
FMECA $\rightarrow$ FTA
Testability Analysis

Testability

Define BIT concept & Tests to calculate
BIT Coverage and Isolation

• Assign for each Failure Mode the Relevant Built-In-Test (BIT)
Testability Analysis

What is it?
• Decision support tool for design of Built In Test (BIT) concept
• Based on FMECA defined failure modes
• Assign Tests and BITS to failure modes
• Calculate coverage and isolation

Why is it important?
• Identify non-covered failure modes
• Identify redundant tests that may reduce isolation
• Good isolation:
  • No “guess work” and replacing of good parts
  • Reduce maintenance time and cost
Define BIT concept & tests
to calculate BIT Coverage and Isolation

- Assign for each Failure Mode the Relevant Built-In-Test (BIT)
Testability Analysis Fault Isolation

If A fails: BIT1, Isolation level 1 (A fail)

If B fails: BIT2, Isolation level 1 (B fail)

If C fails: BIT1 BIT2, Isolation level 1 (C fail)

(but we need to add a super BIT functionality)
Testability Analysis - Assigning Tests

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>Function</th>
<th>Mode name</th>
<th>Testing</th>
<th>BITS and Tests</th>
<th>Next effect</th>
<th>End Effect name</th>
<th>Severity</th>
</tr>
</thead>
</table>

Function failure modes:
- Assign tests for each failure mode.
FTA: Fault Tree Analysis

FTA

Build the Failure Modes Combinations Tree for System Safety Analysis
• Build for each Safety Event the possible causes
• Top-Down Assignment of Logical gates
Fault Tree Analysis (FTA)

What is it?
• Top down analysis of safety event causes
• Based on FMECA defined failure modes + additional external causes (Environment & Operation)
• Assign Logical gates for event combinations (AND, OR…)
• Calculate event probability

Why is it important?
• Required in many industries for Safety analysis of possible catastrophic events
• Sensitivity analysis: identify main contributors to occurrence of safety events
• Can be used for root-cause analysis
Fault Tree Analysis

Build the Failure Modes Combinations Tree for System Safety Analysis

• Build the possible causes for each Safety Event

Top-Down Assignment of Logical gates

FTA Sensitivity analysis:
Find main contributors to safety event:
Fault Tree Analysis: Logical Gates

OR

AND

AND Priority

Standby

NOT

K out of N
RBD
Reliability & Redundancy Block Diagram

- Build Redundancy model
  for System Availability Calculations
- Assignment of required blocks / functions for a mission
- Define the blocks / functions redundancy model
Build Redundancy model for System Availability Calculations

• Assignment of required blocks / functions for a mission
• Define the blocks / functions redundancy model
What is it?
• Analysis of required functions and block for system operation
• Assign redundancies (Serial, Parallel, K out of N…)
• Calculate Availability, Reliability, mean Failure and Repair times

Why is it important?
• During concept stage: Allocation of block failure rates based on required system availability
• Assign redundancies for high availability
• During detailed design: Treat complex cases using
  • Network module
  • Markov chain module
• Calculate SIL level for IEC 61508
Reliability Block Diagram

Redundancy Models

Simple Block (Leaf)
Serial
Parallel
K out of N
Standby
Network
Markov
Reliability Block Diagram
Redundancies

Adding redundancy for a drone as example:

- Nav. Sys: 2x CPU
- GPS: 2x GPS +voter
- IMU: Optic + Mechanical gyros
- Flaps: 2x Motor + Encoder for each flap

Before:
A = 0.899

After:
A = 0.999
Conclusions

• fiXtress™ & CARE® creates the new standard in Digital Reliability Engineering

• Leading tools for EDA engineers

• Integrated with popular EDA tools

• High usability and ROI

• Increases product’s robustness and reliability

• Reduces the design process time and Time To Market

• Cuts design process costs